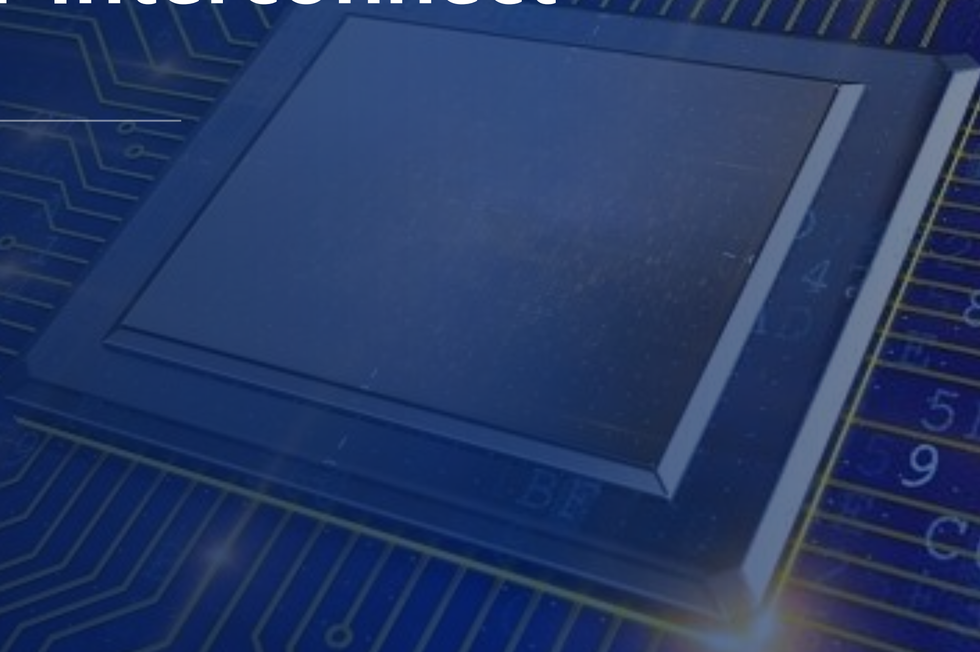
Designing Chiplet-Based 2.5D High-Interconnect Density Semiconductor Packages:

Challenges and Considerations



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CTO D.H. Jayden Kim

HANA Micron Corporate Overview

"HANA Micron is a leading Semiconductor Package Turnkey Solution Provider in Korea"

HANA Micron — HANA Materials — HANA Optronics

OSAT Service	Product	Fab. Equip. Parts	Optical Module
• Bumping • Assembly • Wafer Test • Final Test	• DRAM, eMCP, eMMC • Memory Module • AP, RF, MCU, FPS	• Silicon Electrode & Ring, Ingot • Silicon Carbide Ring • Fine Ceramics Parts	• Automotive LiDAR Module • ToF Module/SiPIC Module • Semiconductor Laser Heater

Customer

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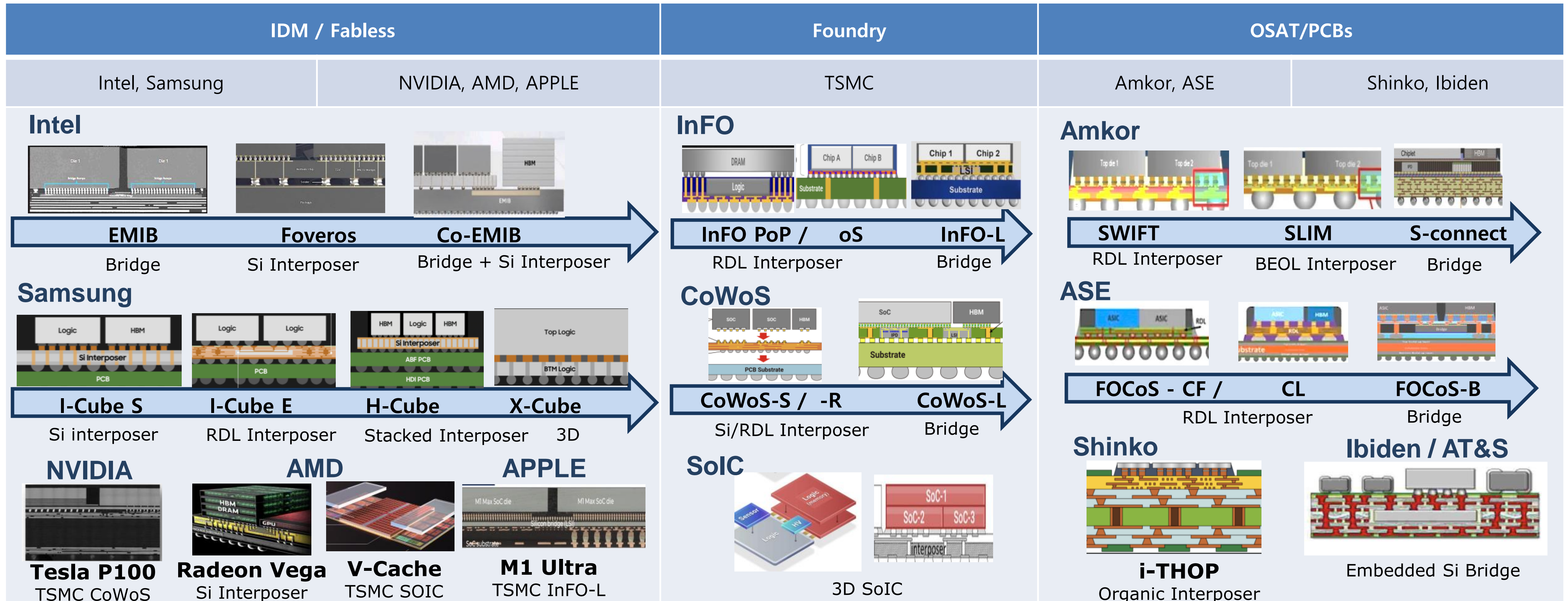
Chiplet Based Advanced Packaging Technology Overview

- **Foundries and IDMs :** Developing in-house and Establishing a Tech. Platform including 3D and 2.5D
  → preventing true heterogeneous integration of chiplets from different foundries.
- **OSATs :** Focusing on Backend 2.5D Integration. Silicon Interposer, RDL Interposer and Silicon Bridge



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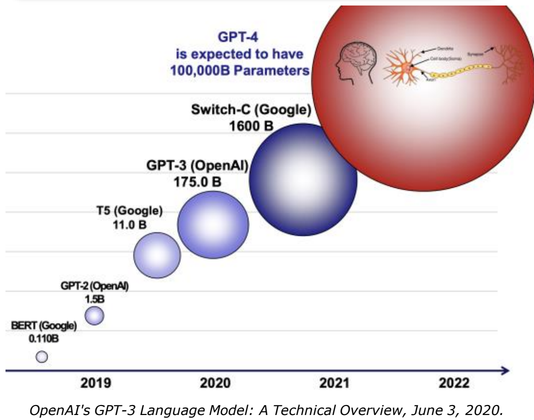
Demand for Interconnect Standard & Low Cost 2.5D Tech. Solution

- **AI Computing Power :** outpaces Moore's law.
  →In-PKG Interconnect standard for lower design cost and OSAT need to develop low cost PKG technology.

Hyperscale AI
Exponential Data Growth



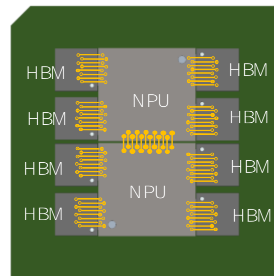
OpenAI's GPT-3 Language Model: A Technical Overview, June 3, 2020.

GPT-3 Training: 3640PFlop/s-days
→ Costs $4.6M Per Training
https://arxiv.org/pdf/2005.14165.pdf

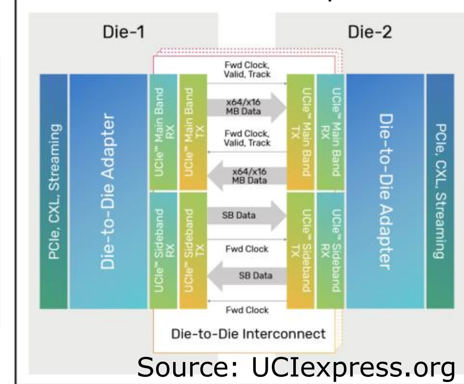
To train it in a day:
→ 29120 x Nvidia V100 GPUs
→ GPU Silicon Area: 250 ft^2, 400 Wfs
→ HBM2 Silicon Area: 580 ft^2, 920 Wfs

PKG High Speed Interconnect
Computing Unit to Computing Unit or to Memory

Near-Memory CPU

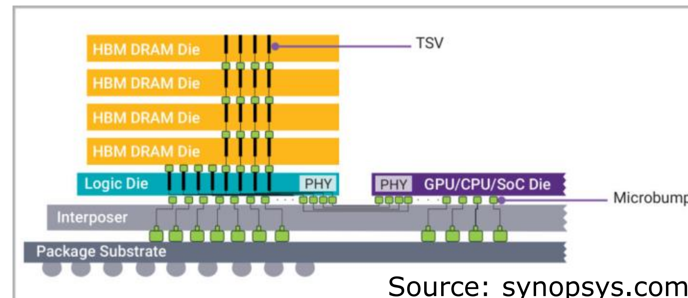


UCIe (Universal Chiplet Interconnect Express)



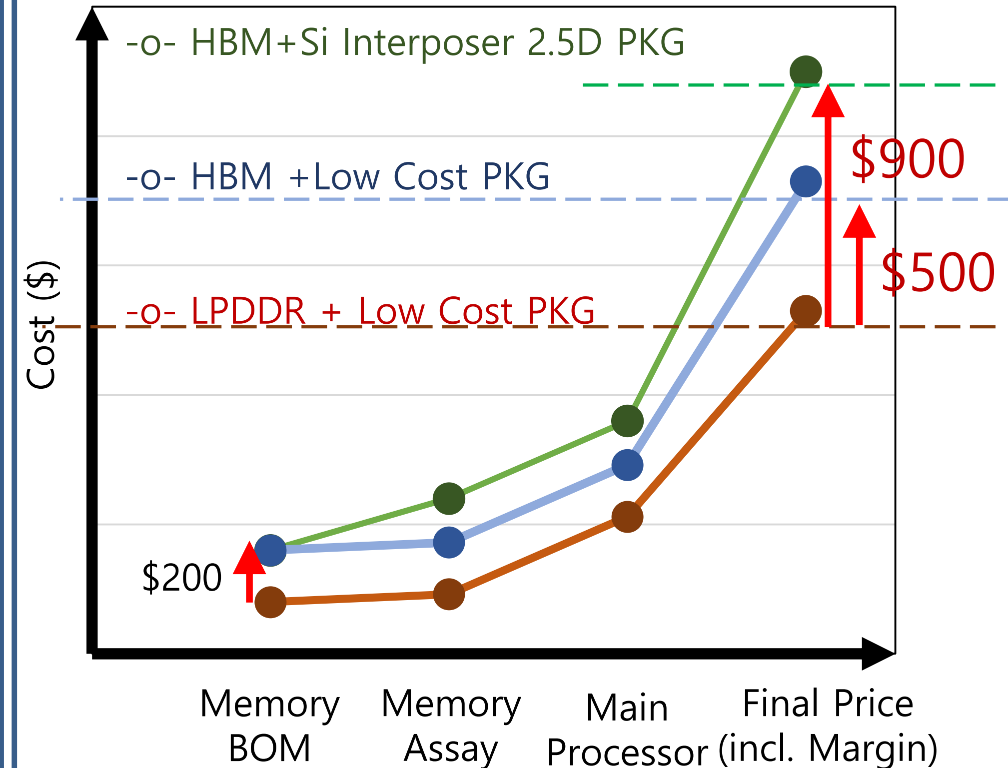
Source: UCIexpress.org

HBM (High Bandwidth Memory DRAM)



Source: synopsys.com

PKG Cost Impact.
NPU Product Cost with 64GB on PKG Memory



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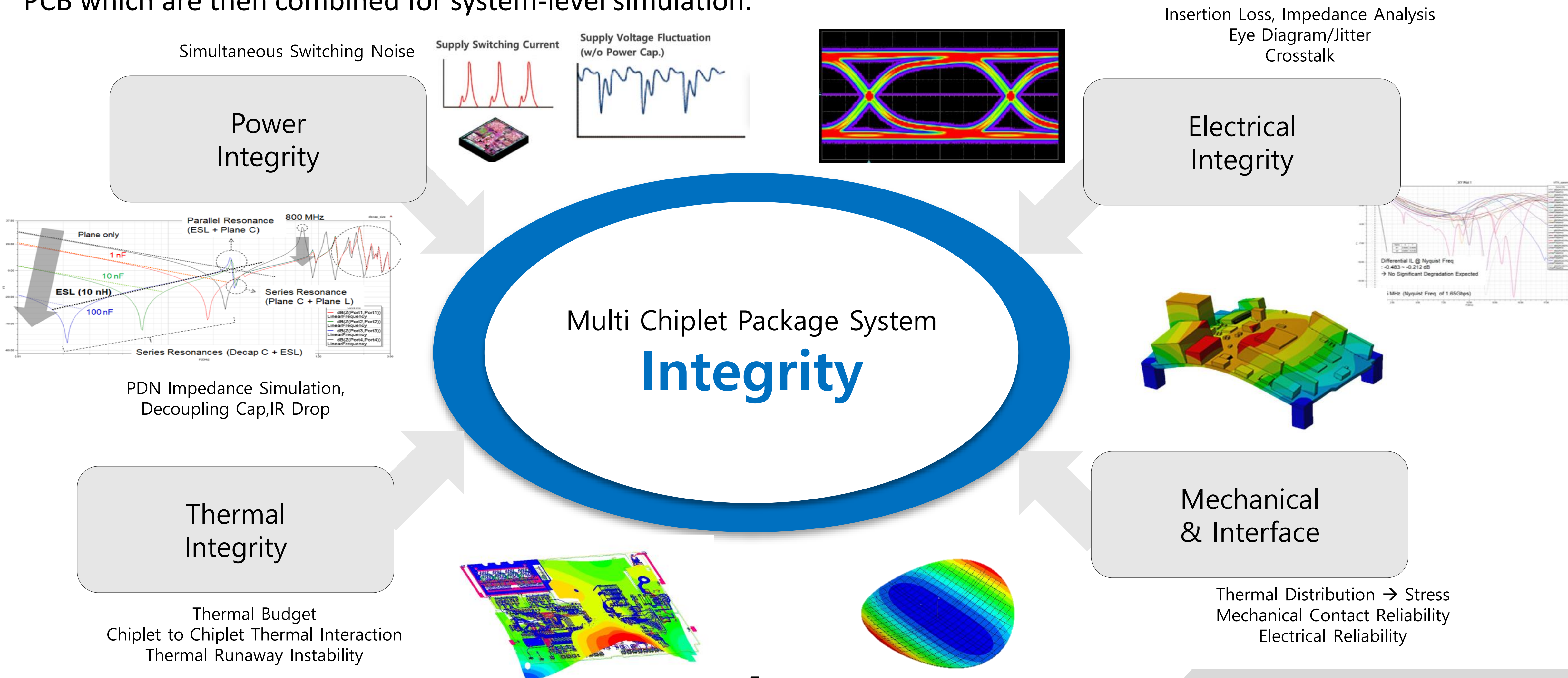
Package Design Verification

☐ Interaction Verification

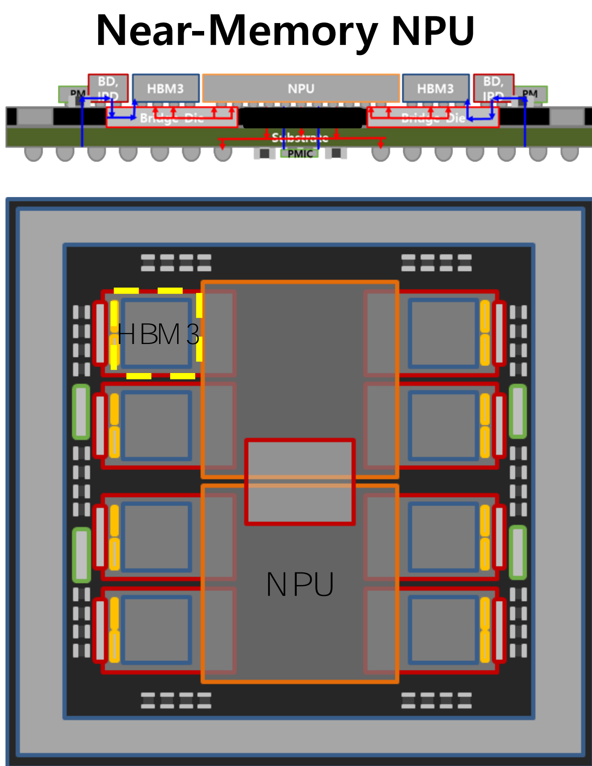
User-friendly design flows require the creation of signal, power, thermal and mechanical models for the IC, package and PCB which are then combined for system-level simulation.

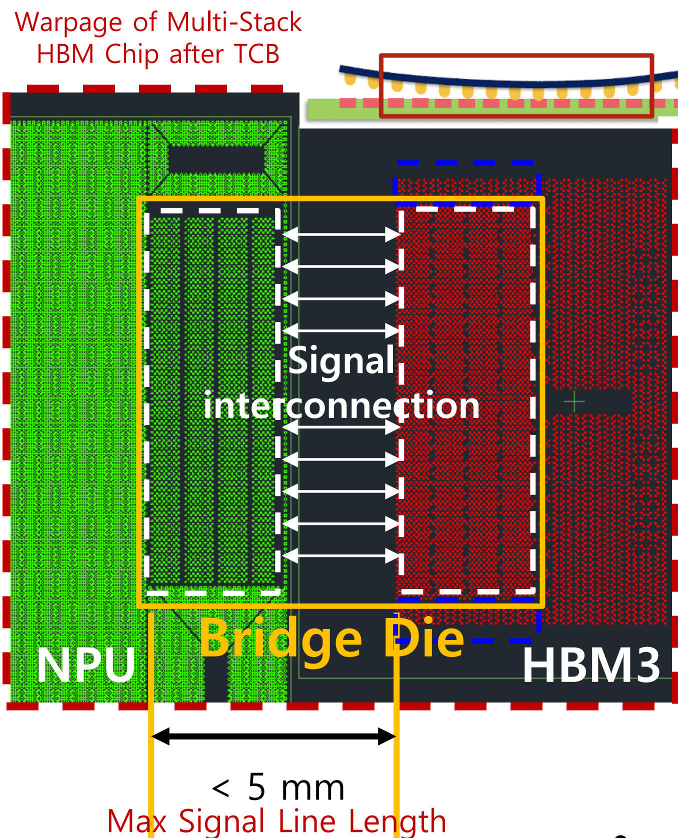


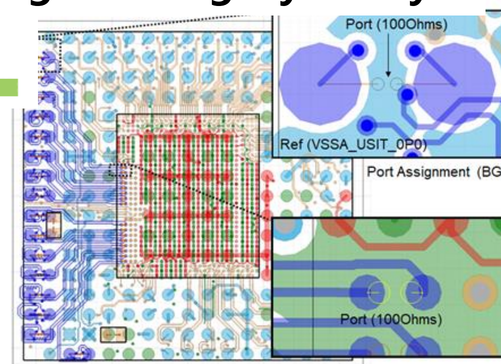
Near Memory NPU – HBM3 Signal Line Design

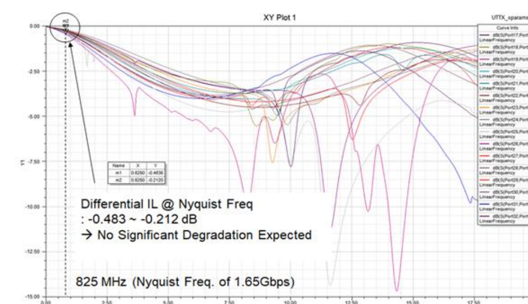
- ☐ **HBM3 chip dimension:** > 3000 I/Os per 8mm Signal Width & max 5mm Signal Line
- ☐ **SI Anlaysis:** due to large insertion loss (Long Signal Line), L/S >2um Signal Line needed.

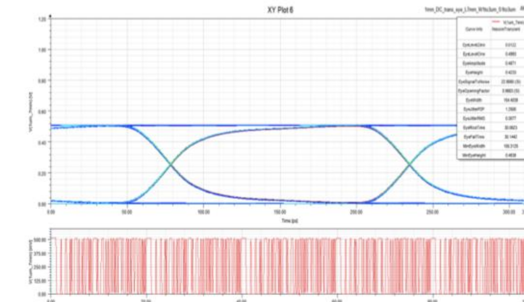
  → Limiting Linear Escape Density to 250 I/O per mm-Layer, SERDES needed for future Gen.

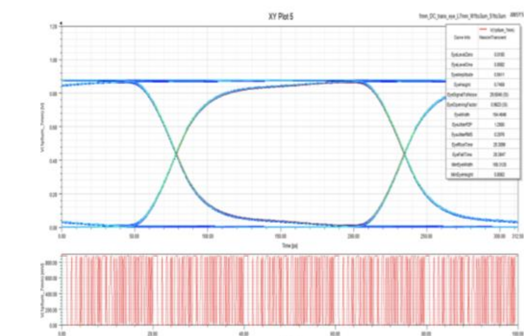












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3D Stacked Memory drastically boost Bandwidth

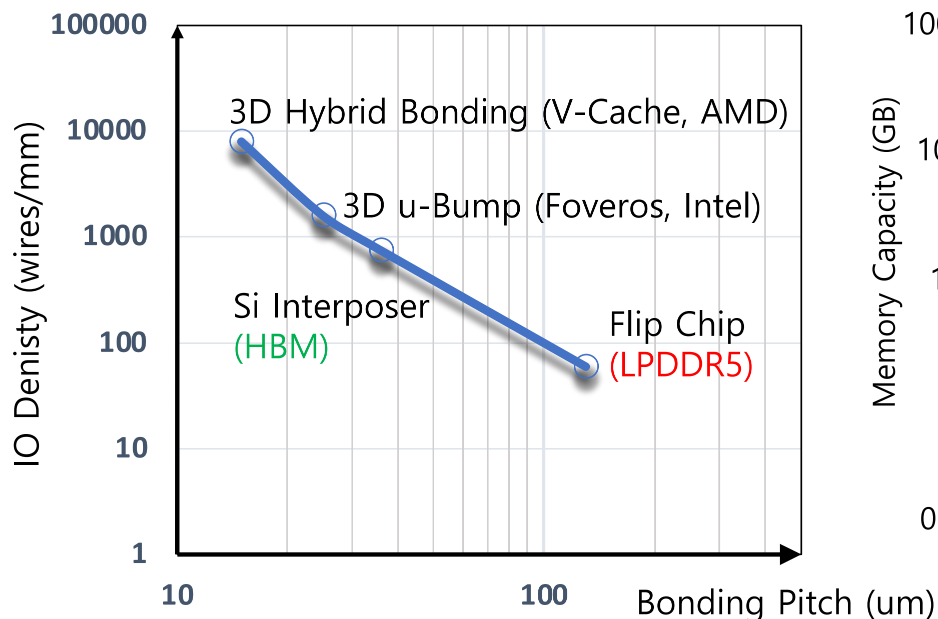
☐ **3D Stacked Memory on Processor:** Highest Memory Bandwidth Possible.

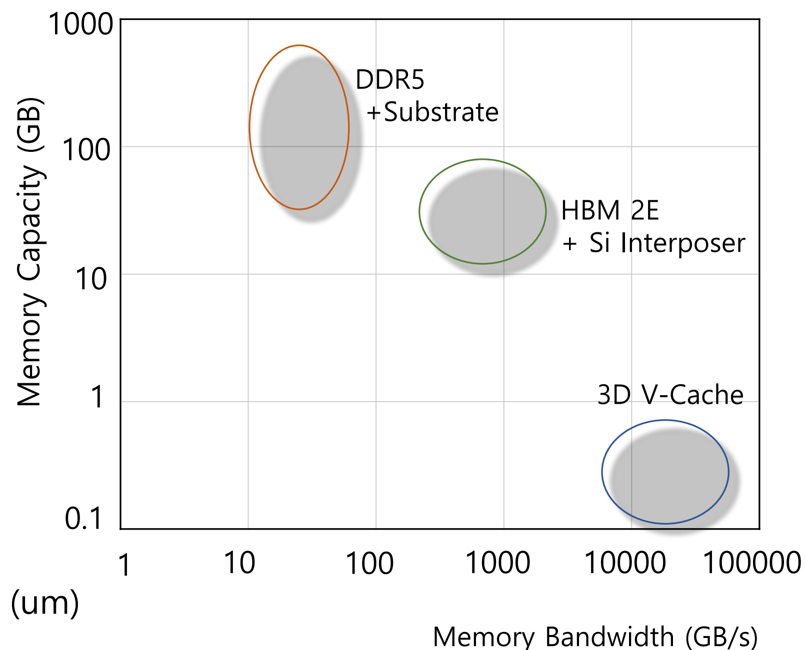
→ AMD's V Cache SRAM: <32MB. Too small for large parameter deep learning.

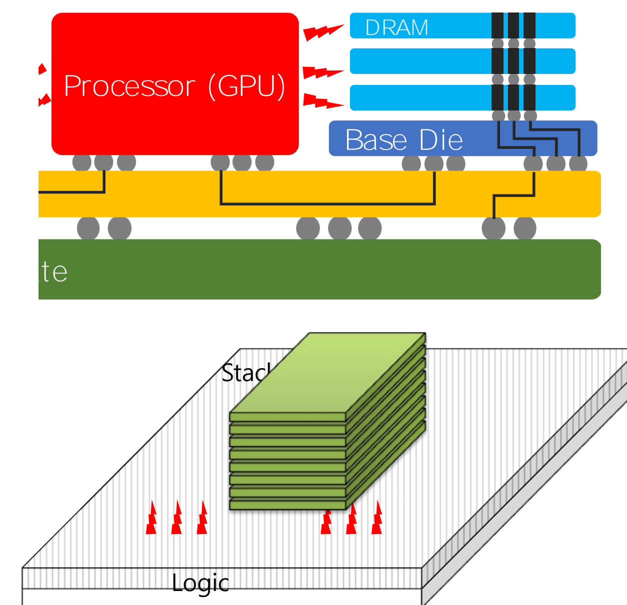
☐ **HBM on Processor or Processor in HBM:** DRAM's operating temperature is limited < 85C°

→ Processing unit's performance is limited by thermal budget.

☐ **High Operating Temperature + High Speed + High Density Memory + High Endurance Needed**







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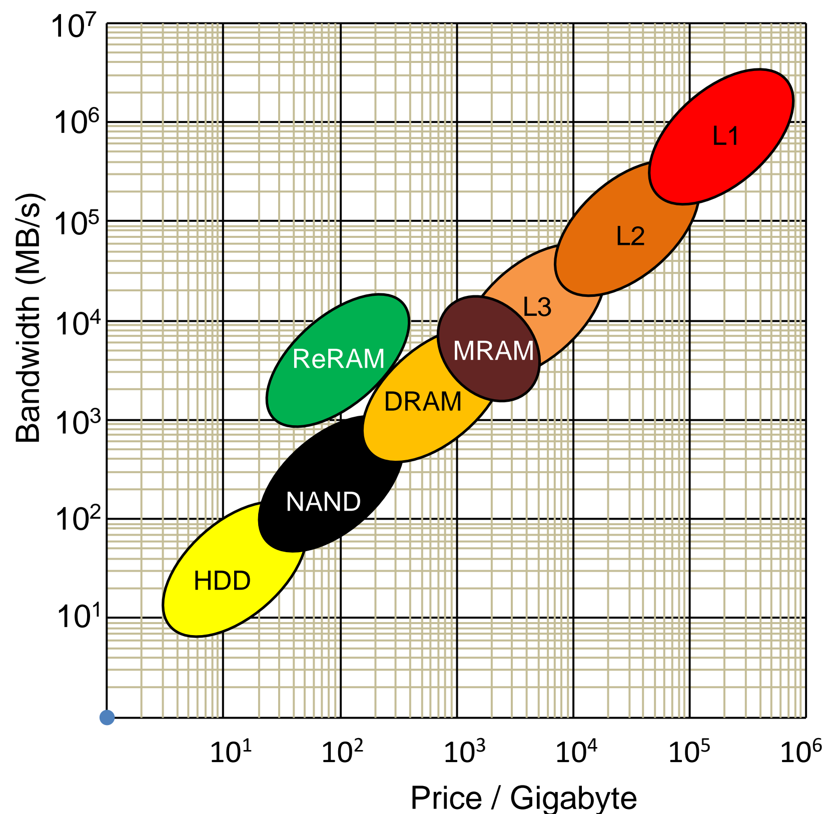
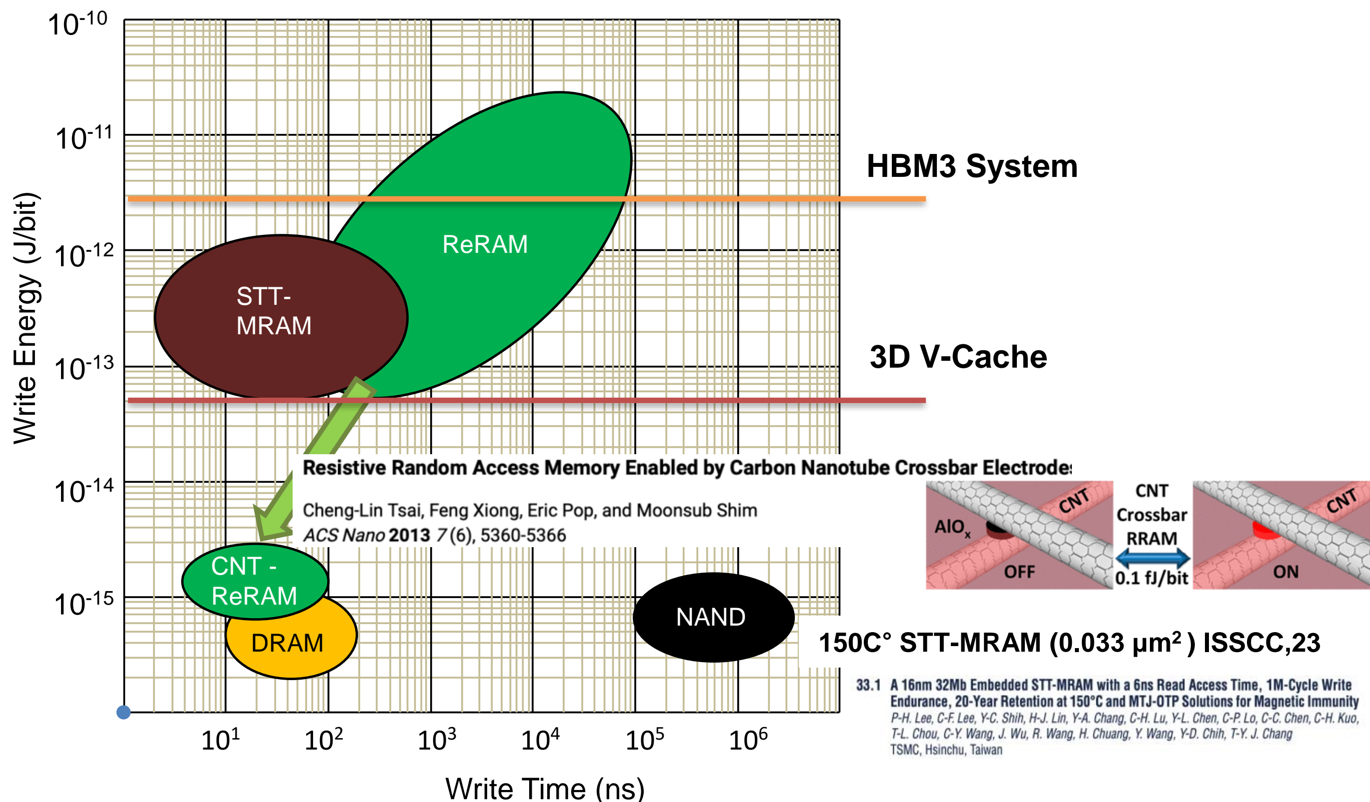
3D Stackable Memory Candidates

- ☐ **MRAM and ReRAM have potentials:** Similar cost and read bandwidth to DRAM.
  - → Nano-technology (ex. CNT) might help reducing the Write Energy.
  - → By sacrificing retention, operating temperature might be increased.
- ☐ **Further New Memory Device Research needed for more efficient AI Processor.**





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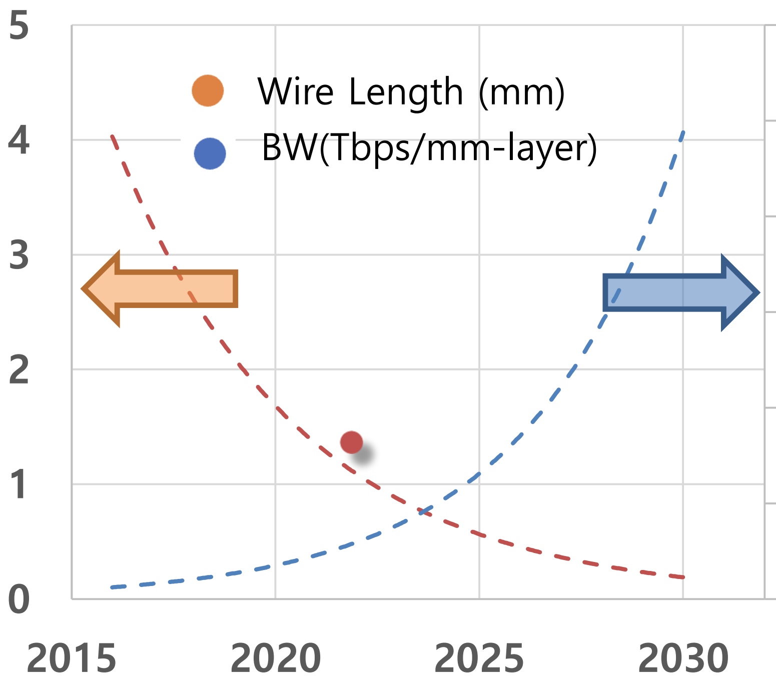
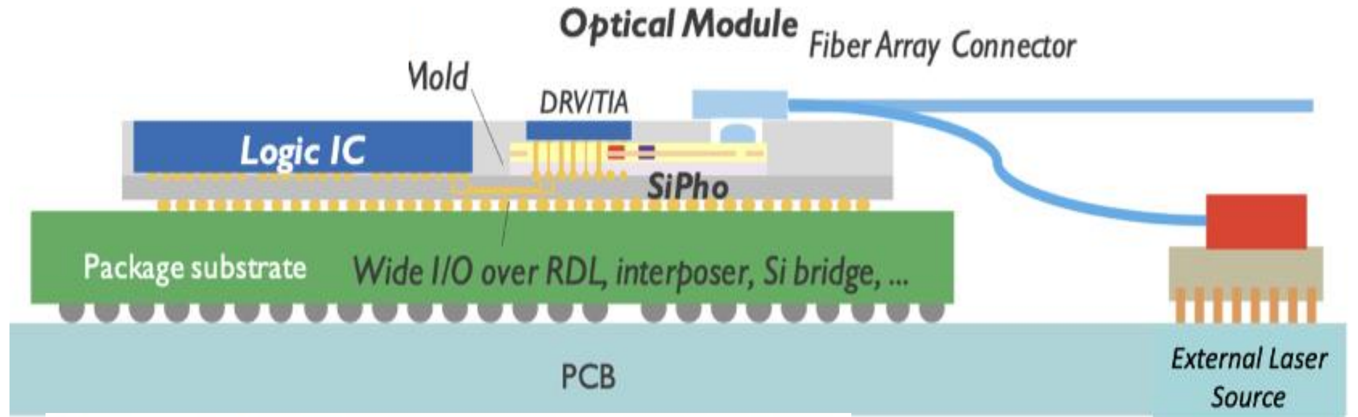
Optical Interconnects between Chip Packages

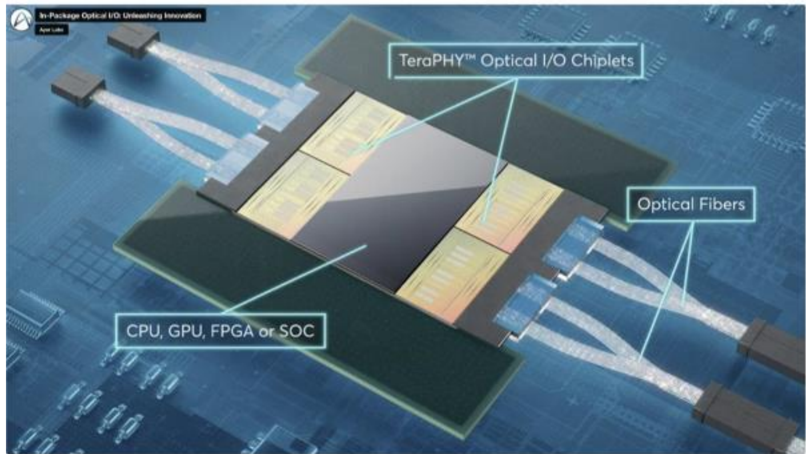
☐ **CPO (Co-Packaged Optics):** Silicon Photonics in Chiplet PKG.

→ Waveguide, Modulator, PD, WDM Filter, DeMux, Coupler etc.

☐ **BW Target: >1Tbps/mm @ distance up to a few km** (w/2.5D requires <5mm short distance)







AyarLabs
TeraPHY™
BW>200 Gbps/mm
Energy <5pJ/b
Range <2km

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Conclusion

☐ OSATs are developing low cost 2.5D Advanced Packaging Technology.

☐ Power, Electrical, Thermal and Stress integrities must be thoroughly examined.

☐ 3D Stacking of Memory to drastically improve the Memory Bandwidth

☐ Novel Memory operating at higher temperature is needed

☐ Optical Interconnect started to be co-integrated in same package.

☐ Collaboration with USA research group played a vital role.

→ Past a few years, worked with USA Universities on optoelectronics projects funded by Korean Government.

→ Collaboration ended due to classification of the project as a National Security Tech.

→ Advanced Packaging Technology is currently classified as a National Core Tech.

☐ In Semiconductor Advanced Packaging Field, NSF and Korea Government Joint Research Program would facilitate further collaboration between two countries.

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